REMARKS

Applicants have amended the claims in order to more particularly define the invention taking into consideration the outstanding Official Action. Applicants have amended claims 31 and 38 as required by the Examiner in the Official Action to correct some minor informalities. Claims 45 and 46 have been added to the application to further define the invention as fully supported by Applicants' specification. As clearly shown in figure 5H, at least one side of the layer is coplanar. Accordingly, it is most respectfully requested that the objection to these claims be withdrawn in view of these amendments.

The rejection of claims 31-44 under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. in view of Ho has been carefully considered but is most respectfully traversed in view of the following comments.

The Murakami et al patent (U.S. 5,866,948) discloses at various portions, including column 4, lines 7-15, fig. 1, the substrate 1 having the through hole 4 is formed with the plating 5, and the chip 2, thereby bonding wires 7 are connected with wiring pattern 3 together to reduce higher cross-talk noise and thermal stress.

The means of the technology:

Shown in figure 8, the chip 2 is thereby bonded with bonding wire 7 to be electronically connected with the bonding pad 13 on the stud 12, wherein the interposer 15 is compressing of the stud 12, bonding pad 13 and the land 14 and, the chip 2 is bonded to the die pad 16 thereon.

Comparison between the way of connection by electronics and the difference of structure:

(1) The chip of the invention is electronically connected to lead layer (as fig. 5H), however the chip of '948 is thereby the wire 7 is electronically connected to the stud which would be understood by one of ordinary skill in the art to be different from the

lead layer of the present invention. And further lead layer is directed to electronically connect to PCB and, the stud of '948 is extruded from the substrate thereby land is electronically connected with PCB together.

(2) The die pad and the solder mask and the layer of conductor in the invention are parallel whereon is located and, the die pad and solder and lead layer in '948 are all extruded from the substrate. They are not coplanar in accordance with the present invention. There is no motivation in the prior art, absent Applicants' disclosure to provide the necessary motivation to modify the reference to arrive at the presently claimed invention. Moreover, obvious to try is not the standard to obviousness under 35 USC 112.

(3) In addition, '948 does not disclose another embodiment of the invention, which the die pad of the invention as fig. 6 could be the solder mask and, the chip is electronically connected to lead layer. These are claim limitations which cannot be ignored.

II. U.S. 6,455,926 the real structure of the technology of invention

Prior art:

According to the disclosure at column 2, lines 53-57, the use of drilling mechanically on the laminate substrate caused by the loss of time and the increase of cost.

The means of the technology:

Shown in figure 1, metal substrate 14 having hole there into is forming the cavity 28 and, the chip 16 is located there into, wherein the substrate 12 with the use of BUM (Build-Up Multilayer) is forming the signal layer 20 and ground (or power) layer.

Comparison between the difference of purpose and the difference of structure:

(1) The purpose of the invention relates to the improvement of the flash of which the bottom surface of the L/F of the QFN caused, however, the purpose of '926 relates to the improvement of which the use of drilling mechanically on the laminate substrate caused the loss of time and the increase of cost.

(2) The structure of the presently claimed invention is characterized by providing an interim substrate whereon the surface is formed with the solder, lead layer and the chip base and then, the interim substrate is removed after the package forming thereon. However, the structure of '926 is that the substrate with the use of BUM (build-Up Multilayer) is forming the signal layer and ground (or power) layer.

III. The difference of manufacturing process between the invention and U.S. 5,866,948

(1) The following steps of the invention is first setting up an interim substrate made of metal plate as a carrier to provide plating the interim substrate with conductive materials to form a lead layer and die pad layer and then, performing die bonding, wire bonding in and molding processes and further producing a single unit, the package and finally, etching the interim substrate to get a semiconductor package without substrate.

(2) The following steps of '948 regarding to the process of fig. 9 is that first providing a plated layer treated as a mask and then, etching a opening on the metal plate to fill up the epoxy resin therein. These differences in process result in a different structure in accordance with the claimed invention. Accordingly, it is most respectfully requested that this rejection be withdrawn.

In view of the above comments and further amendments to the claims, favorable reconsideration and allowance of all of the claims now present in the application are most respectfully requested.

Respectfully submitted,
BACON & THOMAS, PLLC

By: Richard E Fichter
Richard E. Fichter
Registration No. 26,382

625 Slaters Lane, 4th Fl.
Alexandria, Virginia 22314
Phone: (703) 683-0500
Facsimile: (703) 683-1080
REF:kdd
A04.wpd
July 23, 2003